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Performance of a 512 x 512 Gated CMOS Imager with a 250 ps Exposure Time

A. T. Teruya, S. P. Vernon, J. D. Moody, W. W. Hsing, C. G. Brown, M. C. Griffin, A. S. Mead, V. Tran

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Disclaimer

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Lawrence Livermore National Laboratory

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Collaborators

- LLNL
  - Elden Abels, Rich Bionta, Warren Hsing, Jim Moody, Ted Perry, Harry Robey, Vern Rekow, Alan Teruya, Steve Vernon, Franz Weber
- Massachusetts Institute of Technology - Lincoln Laboratory (MIT-LL)
  - Bob Berger, David Craig, Dennis Rathman, Bob Reich, Antonio Soares
- National Security Technologies, Inc. (NSTec)
  - Chris Brown, Matt Griffin, Kris Larsen, Andy Meade, Vu Tran, Pete Torres

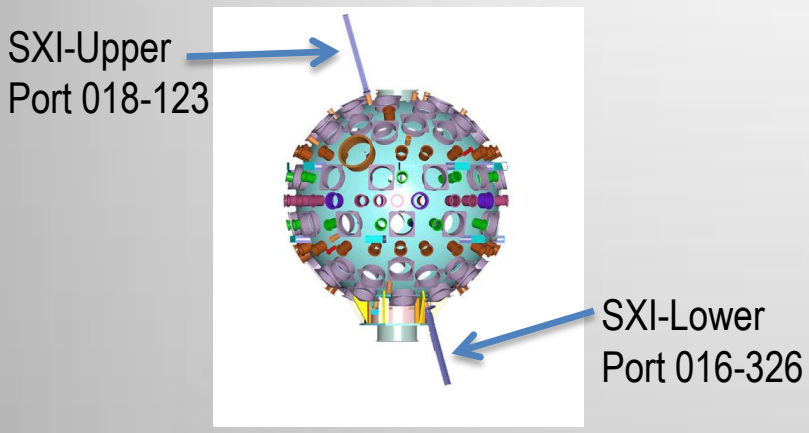
Outline

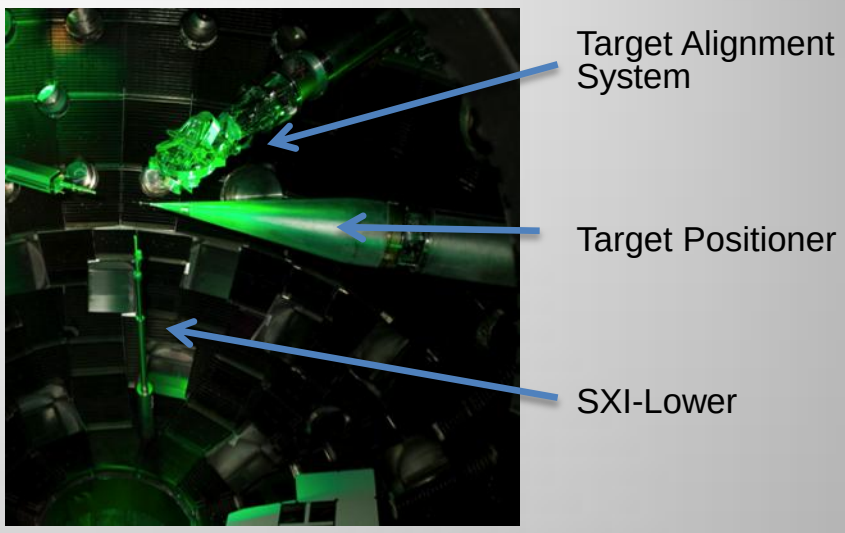
- NIF applications for gated x-ray imaging
- Requirements for a solid state sensor
- Multi-frame, solid-state gated imager conceptual design
- 64x64 pixel prototype characterization
- 512x512 imager concept
- ROIC characterization
- X-ray sensor design and fabrication concepts
- Future work

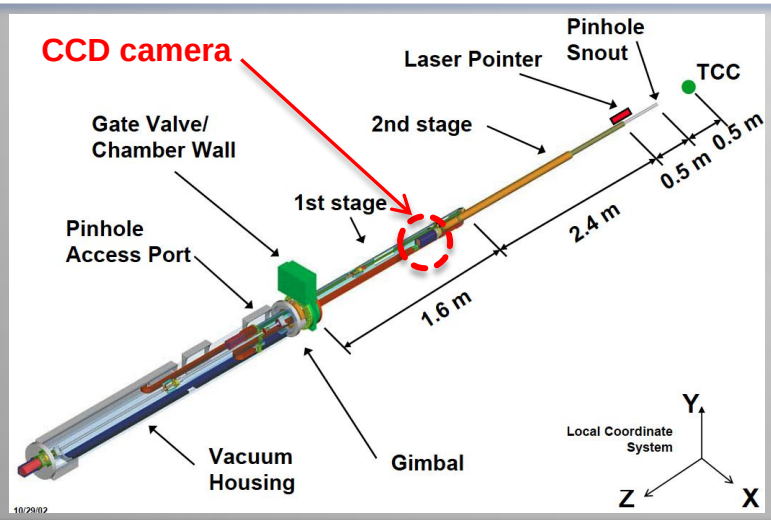
NIF has a need for gated imaging

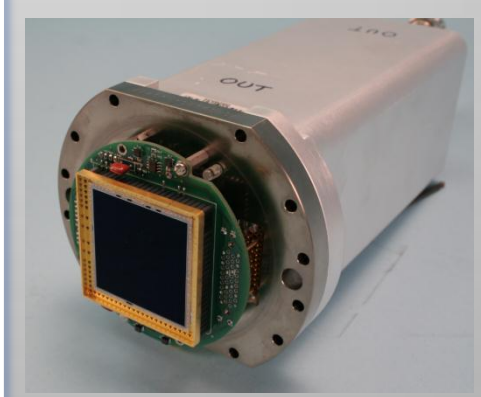
- Current imaging technologies used by LLNL
  - Time integrated – No temporal information
  - Gated – Complicated and difficult to calibrate and maintain
- MIT-LL has developed CMOS technology that can trigger an imaging sensor with sub-ns gates
- Testing is done at the <100 ps Short Pulse Laser (SPL) and ~100 ns Long Pulse Laser (LPL) laboratories, at NSTec - Livermore Operations

The Static X-Ray Imager takes X-ray pinhole images





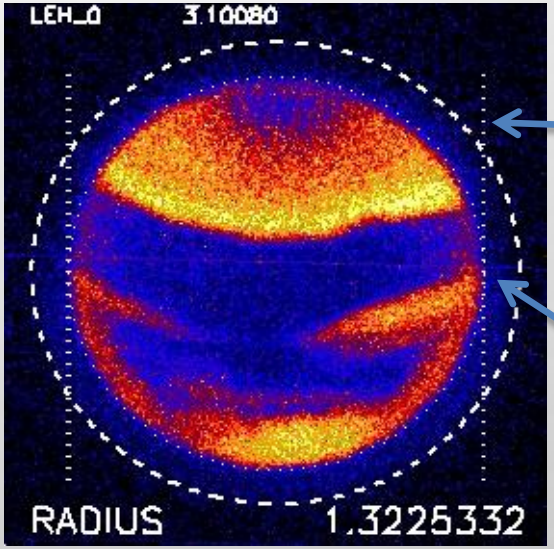




- **SXI X-Ray Camera**
  - Modified Spectral Instruments SI-800
  - Back illuminated CCD
    - 49 x 49 mm
    - 2048 x 2048 pixels
    - 24 x 24 μm pixels
  - ~ 0.7 – 8.0 keV

SXI measures the laser entrance hole (LEH) size to correct X-Ray emission measurements by other diagnostics

Experimental SXI image
1 MJ shot, 3-5 keV channel



Original LEH (dotted circle)

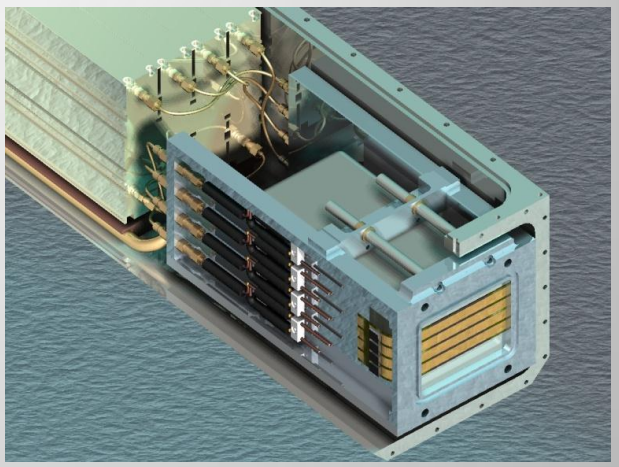
Measured LEH

- SXI provides a time integrated image of the LEH aperture
- Gated images would provide a better measurement of the clear aperture as it varies in time

Image courtesy of Marilyn Schneider, LLNL

A gated imager provides time resolved X-ray pinhole imaging of imploding cores

- Gated X-ray Detector (GXD)
  - Spectral sensitivity from 200 nm to 17.5 keV
  - Four 7.5 mm strip lines
  - Temporal window adjustable 200 -1500 ps
  - Independent gain, gating for each strip
  - Spatial resolution ≤ 60 μm at image plane



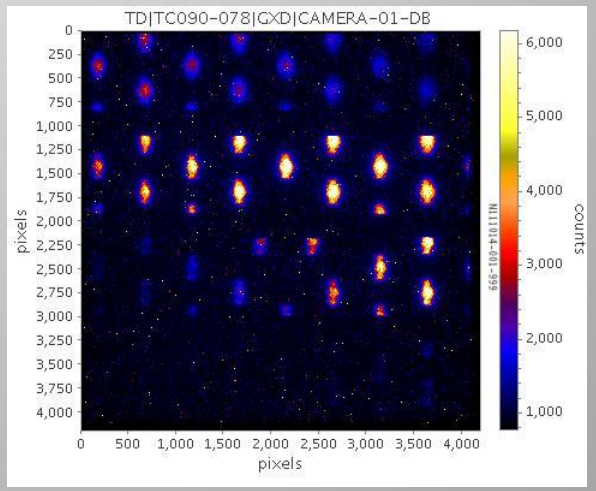


Image courtesy of Steve Glenn, LLNL

Requirements for a solid state sensor

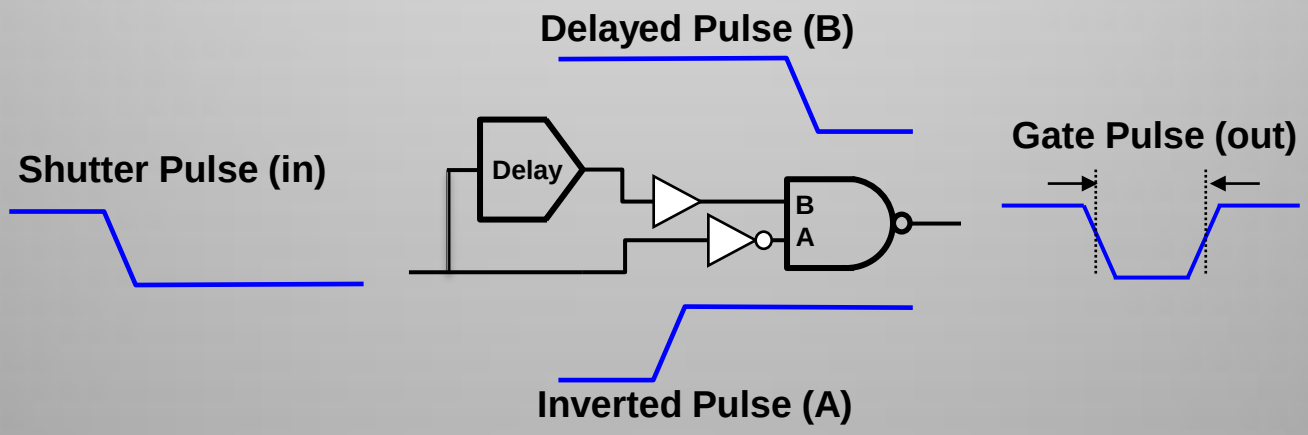
- Need a user selectable gate duration varying between ~10 ps and 1 ns
- Applications require spatial resolution of 20 μm (10 μm is better) at the target (typical magnification is 2x for SXI, 4x to 15x for other diagnostics)
- All applications require multiple frames, preferably taken along a single line of sight
- Experiments require imaging at X-ray energies from 1 keV to 50 keV

Technology development plan

- Development of a CMOS readout integrated circuits (ROIC)
  - Selectable gate lengths
  - Multiple frames
  - Two stages
    - 64 x 64 prototype to test gate distribution
    - 512 x 512 ROIC
- Development of application specific sensors
  - Bump bond sensor arrays to ROIC

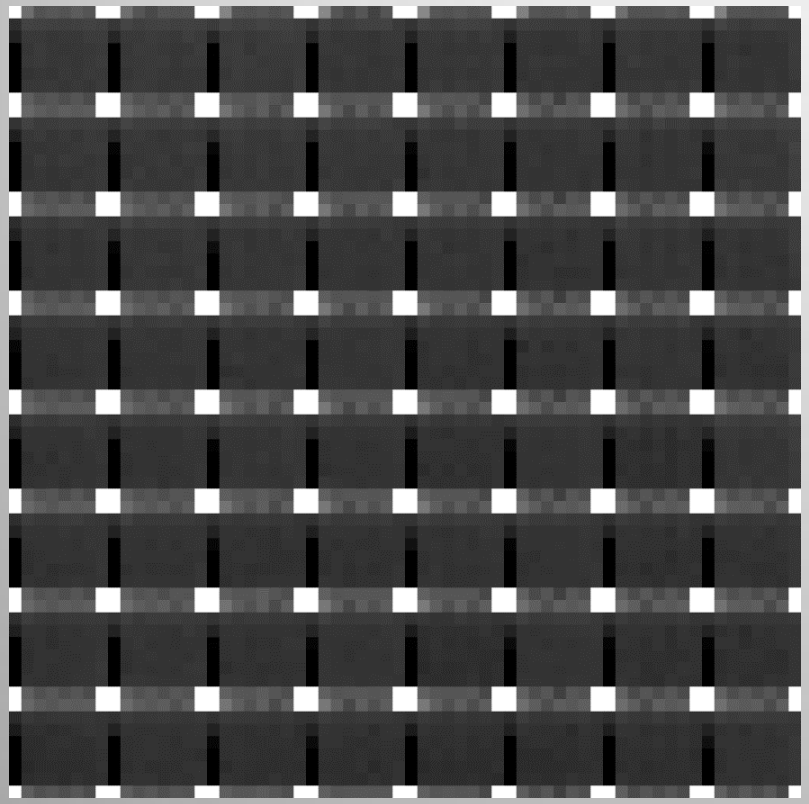
64 x 64 pixel prototype demonstrated trigger distribution and gate generation

- H-Tree structure distributes gate trigger to 8x8 pixel neighborhoods with low skew
- Pulse delay and NAND gate circuitry in each 8x8 neighborhood locally generates a gate pulse of desired length



Architecture of the 64x64 prototype

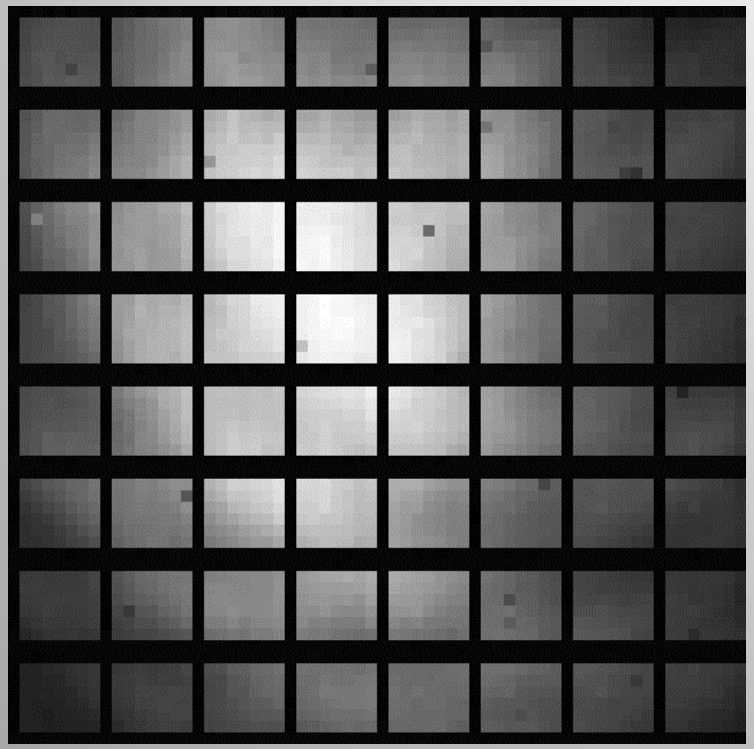
Test Chip Layout (Background image)

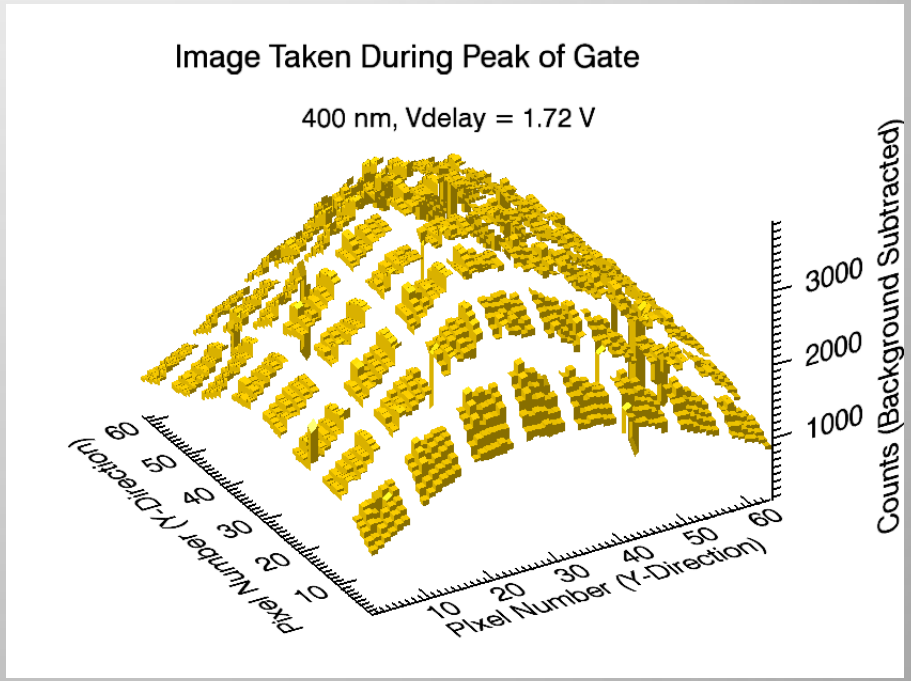


- 8x8 pixel neighborhoods contain 6x7 sensor pixels surrounded by test structure pixels
- Test structure pixels are set to known voltages or currents

Optical tests of the 64x64 pixel prototype with a 200 fs laser validated low skew

Illumination with a 400 nm ~ Gaussian beam (t_{pulse} ~ 200 fs)

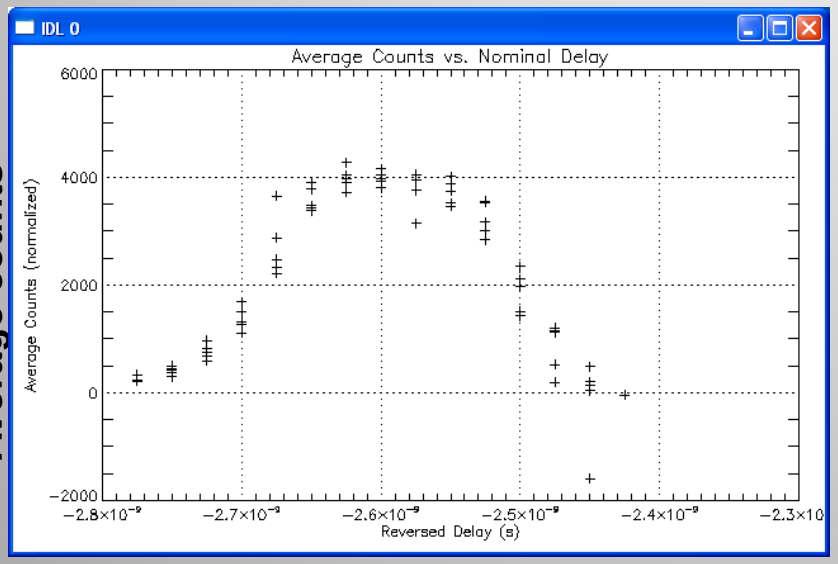




Optical tests with a 200 fs laser validated local gate generation

- **Illumination with a 400 nm ~ Gaussian beam (t_{pulse} ~ 200 fs)**
- **Gate length set by analog voltage V_{delay}**

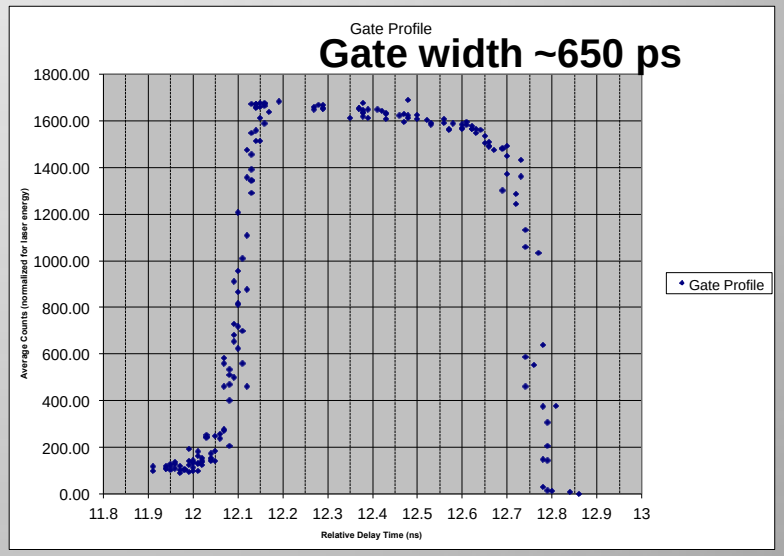
V_{delay} = .5 V



Average counts

100 ps/ major division

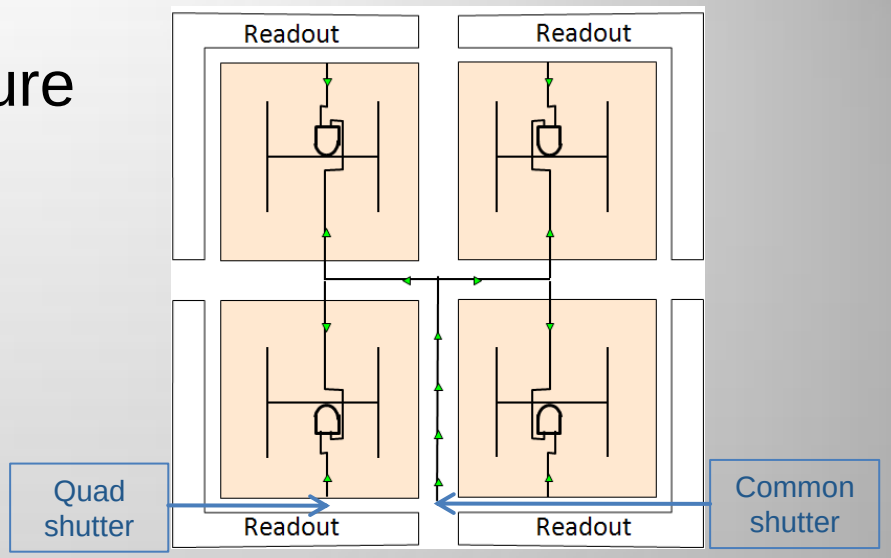
V_{delay} = 1.7 V

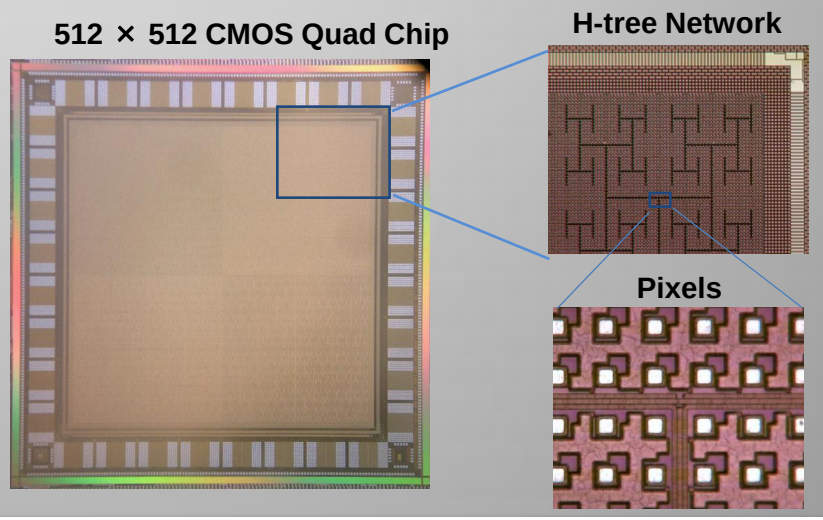


Demonstration of local generation of ~ 200 ps to ~650 ps gates

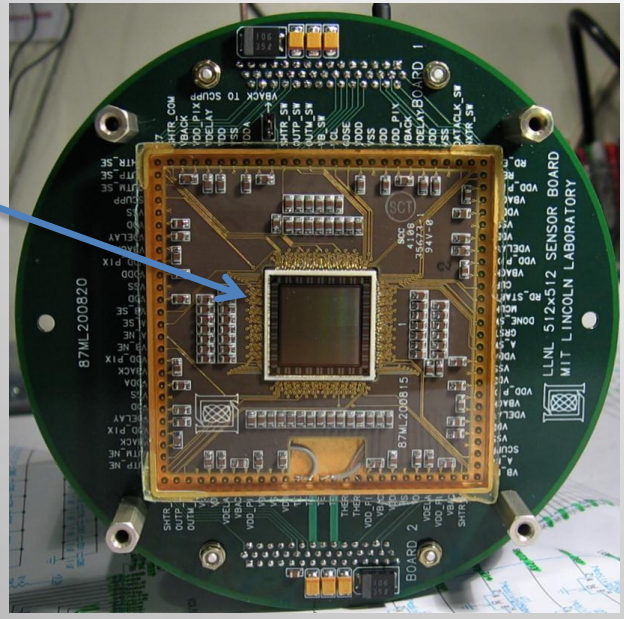
Success of the prototype led to development of a 512 x 512 ROIC

- 8x expansion of H-tree structure
- 4 quadrants may be triggered independently or in common
- Pads for bump bonding photodiode array
- Photosites for optical testing
- Design Specifications
  - 30 μm pixel
  - Fill-factor
    - <10% on-chip
    - >90% bump bonded
  - Timing
    - Jitter <50 ps
    - Skew <100 ps

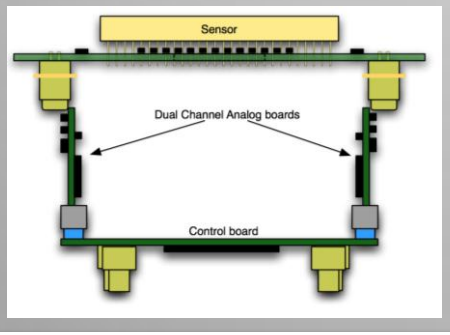




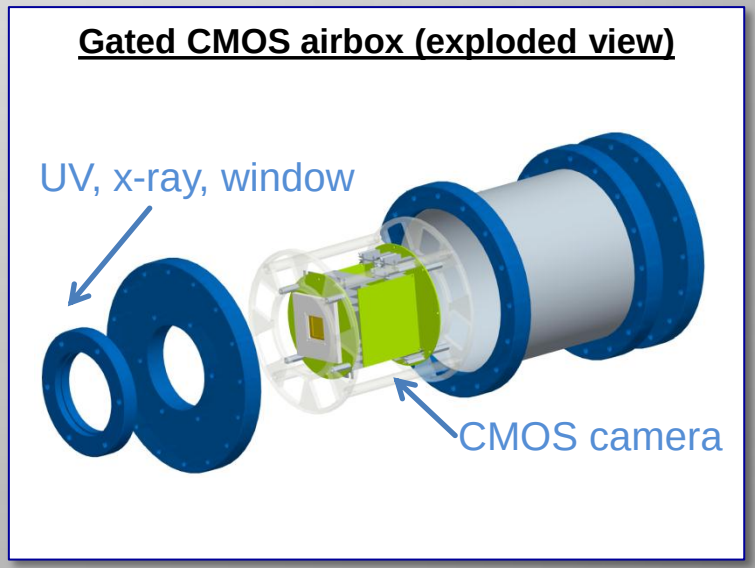
The ROIC was integrated into a custom camera



- Each quadrant has is read out by an ADC
- A housing allows thermoelectric cooling in a dry nitrogen atmosphere
- A photosite built into each pixel allows testing with UV or X-ray illumination



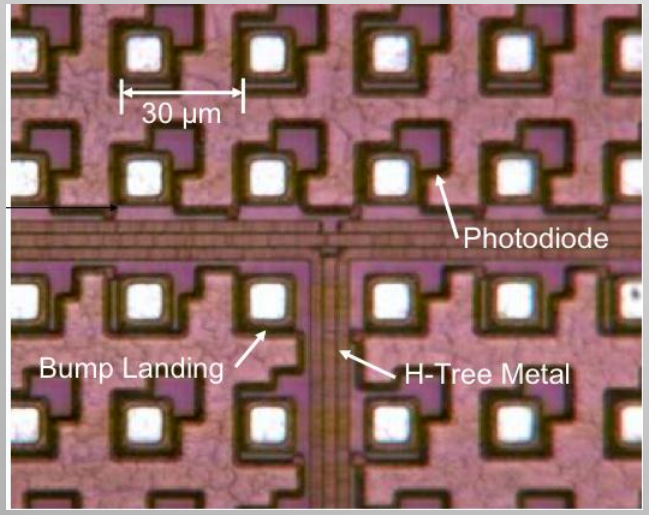
Side view

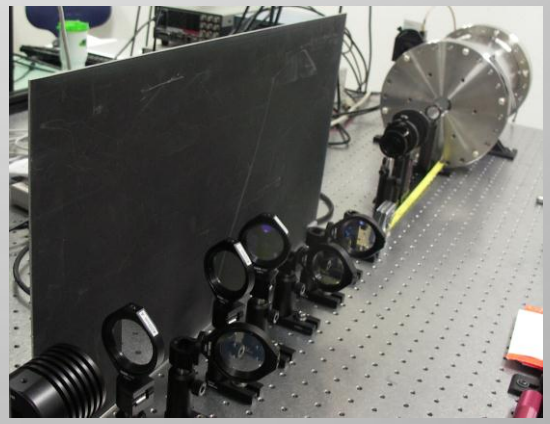


Gate profile measurements

- **A frequency-doubled (400 nm) 50 fs Ti:sapphire laser system was used to measure the gate profile**

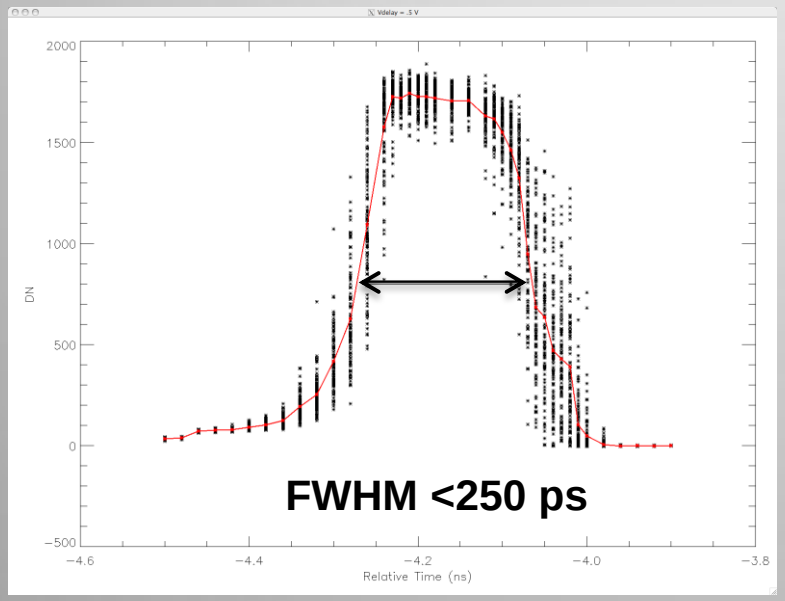
- **The measurement was made by varying the delay time between the shutter trigger pulse and the arrival of the laser pulse at the sensor**



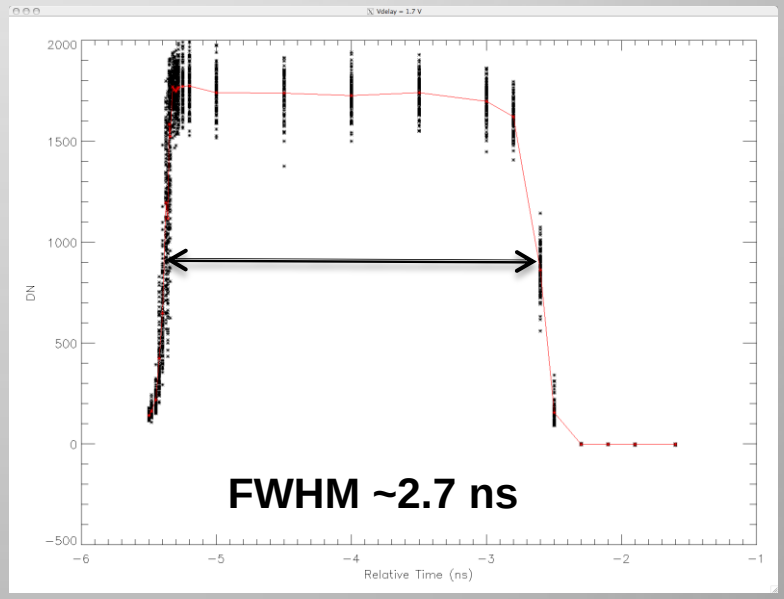


Gate profiles of 512 x 512 ROIC

- Gate profile measurements were taken at the minimum and maximum values for V_{delay} = .5 and 1.7 V
- The short pulse laser lab timing system has an RMS jitter of ~25 ps
- Amplitude noise is higher than would be indicated by laser pulse energy measurements
- Further work is being done to understand sources of jitter and noise in the measurement



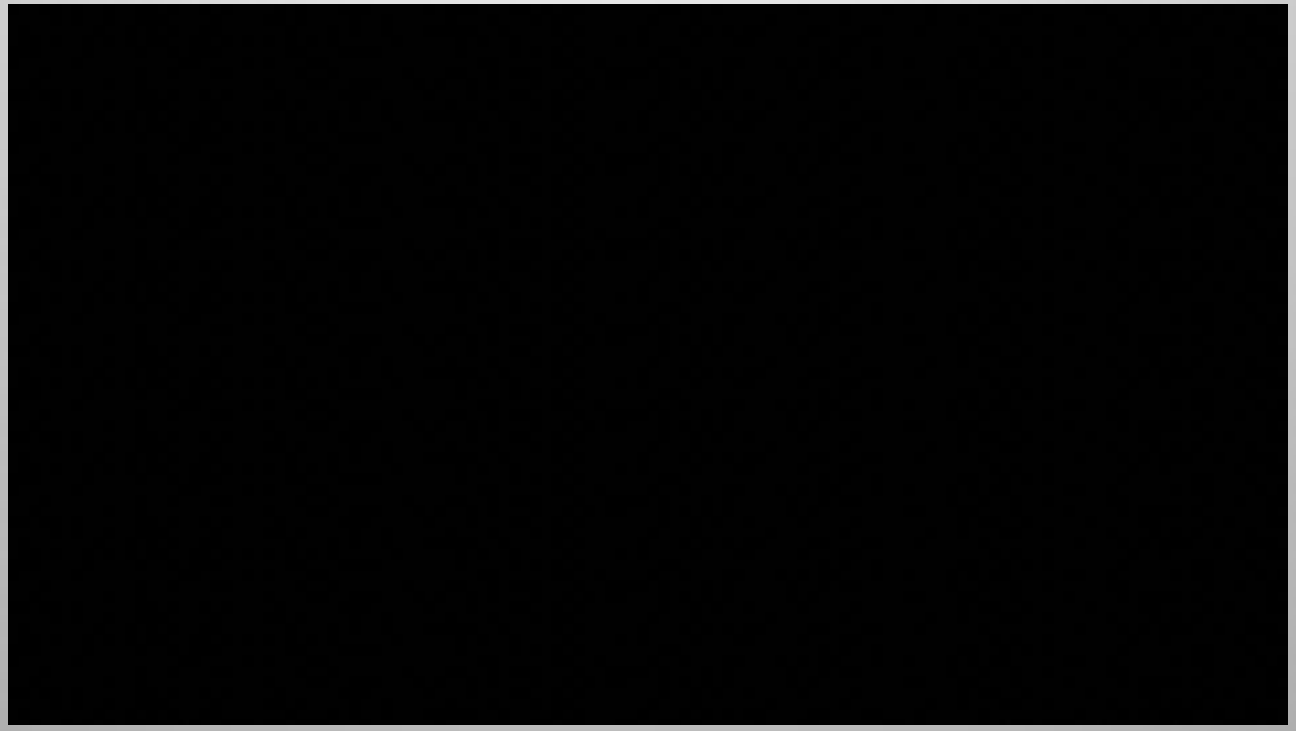
V_{delay} = .5 V



V_{delay} = 1.7 V

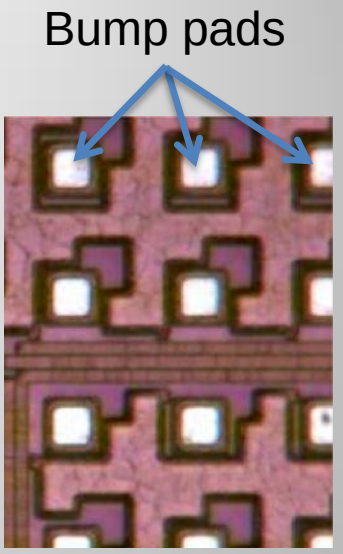
Independent gating demonstration

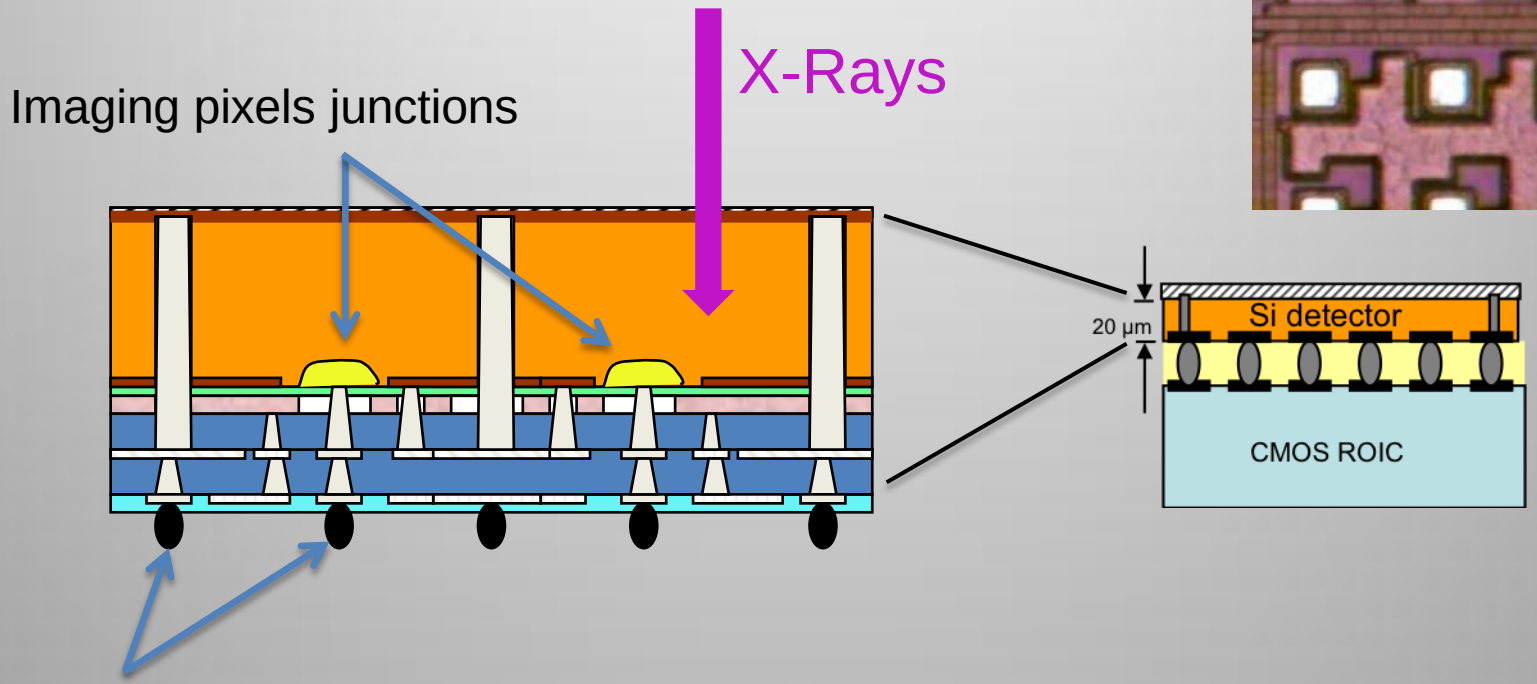
- Independent triggering with 100 ps delay between quadrants
- Laser/sensor timing delay in 50 ps steps



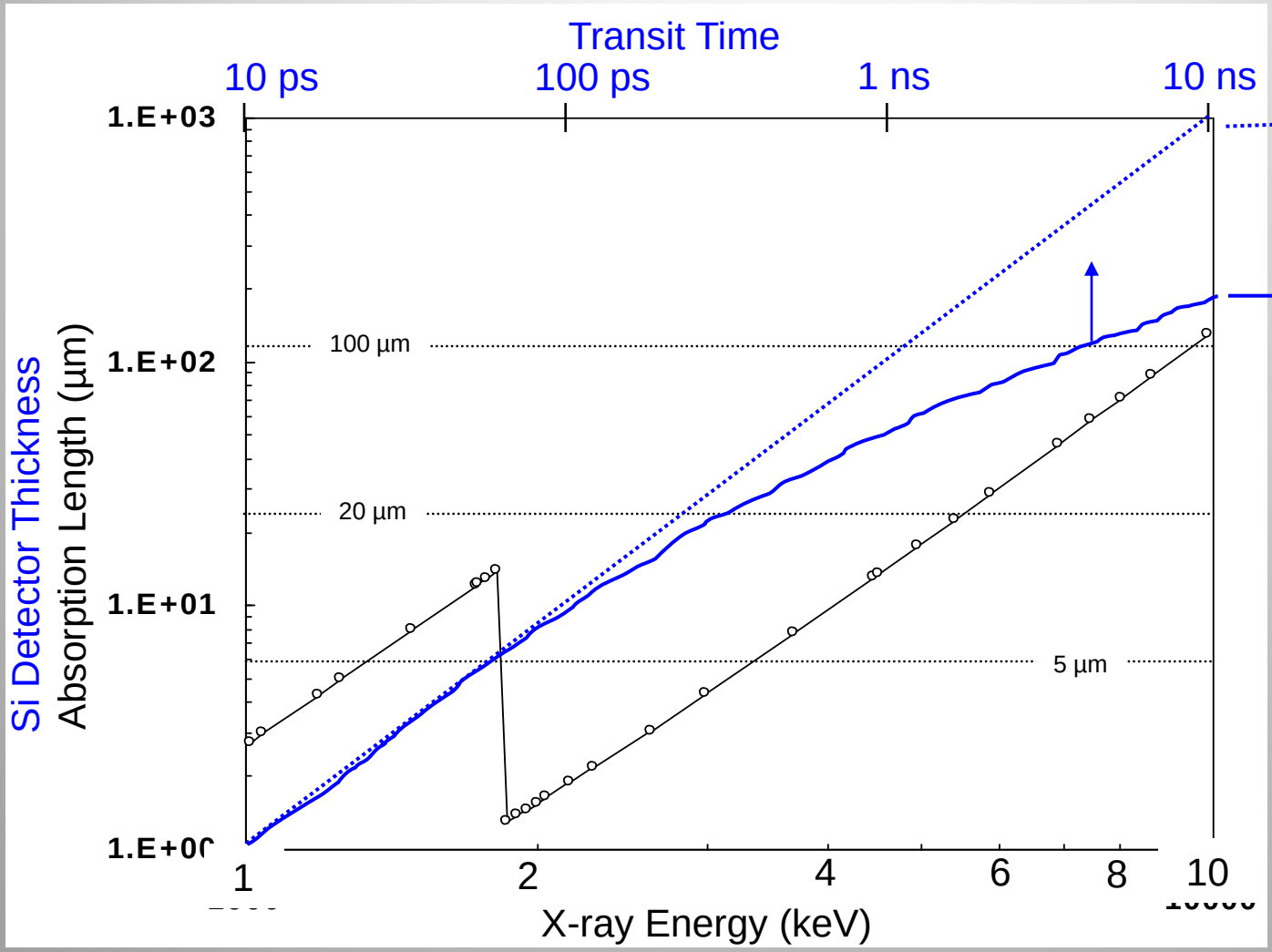
Detector array can be application specific

- Response determined by diode thickness
  - Thinner substrate provides faster response
  - Thicker substrate needed for better QE
  - Fast phosphors may be needed for > 10 keV





Detector thickness determines speed and detector efficiency



Summary

- A gated CMOS ROIC was developed for NIF imaging applications
- A 64x64 prototype tested the H-tree and variable gating concept
- A 512x512 ROIC extended the H-tree and demonstrated independent quadrant triggering

Future Development

- Detector array
  - Looking at options for fabricating an X-ray detector array and bump bonding to the ROIC
  - An associated project is looking at multi-frame pixel version of the ROIC allowing true-single line-of-sight imaging.

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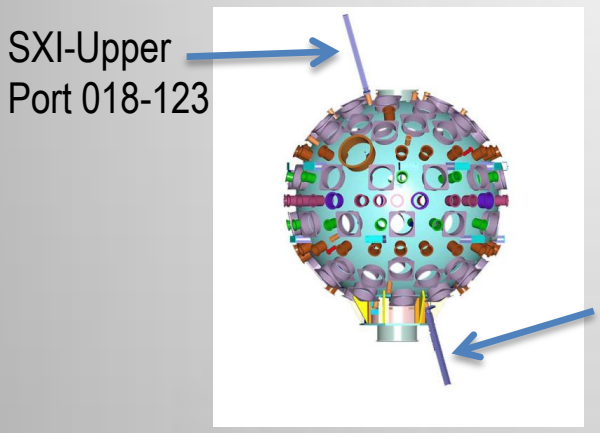
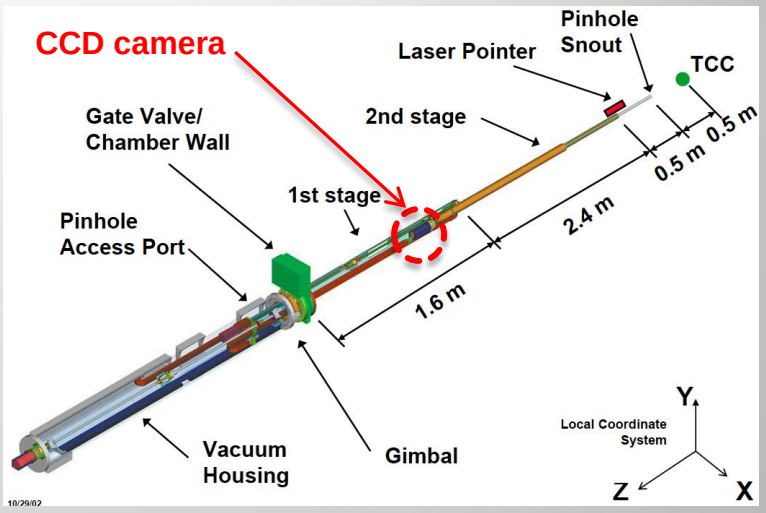
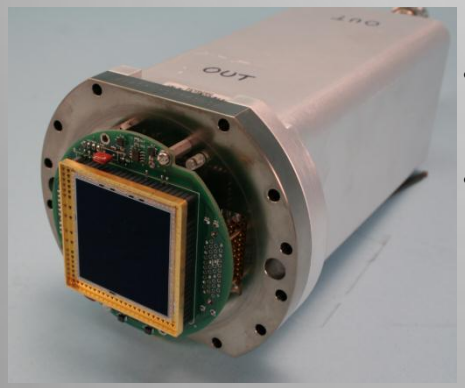
Backup and Alternate Slides

The Static X-Ray Imager (SXI) takes X-ray pinhole images

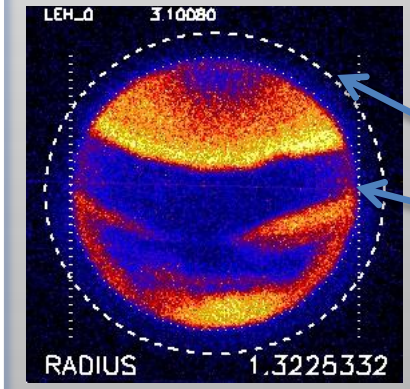






SXI X-Ray Camera

- Modified Spectral Instruments SI-800
- Back illuminated CCD
  - 49 x 49 mm
  - 2048 x 2048 pixels
  - 24 x 24 mm pixels
- ~ 0.7 – 8.0 keV



Laser Entrance Hole (LEH) Measurement

Original LEH (dotted)

Measured LEH

Gated images would provide a better measurement of the laser entrance hole aperture as it varies in time